



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,716	07/21/2003	Luan C. Tran	MI22-2357	7564
21567	7590	02/23/2005	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			KENNEDY, JENNIFER M	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/624,716	TRAN, LUAN C.
	Examiner	Art Unit
	Jennifer M. Kennedy	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 21 July 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 53-61 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 53-61 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/21/03 11/12/03 3/10/04
4/16/04 11/17/04
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 53-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (U.S. Patent No. 5,946,568) in view of Huster et al. (U.S. Patent No. 6,242,329).

In re claim 53, Hsiao et al. disclose the method of forming a DRAM comprising:
forming a first wordline (34, 36) and a second wordline (34, 36) over a substrate,
each wordline comprising a pair of opposing sidewalls (see Figure 5, wherein the
leftmost gate is considered to be the first wordline, and the gate adjacent to the
isolation, and closest to the first wordline is considered the second wordline;

defining four nodes proximate the wordlines, the four nodes comprising a first
node (leftmost 44B), second node (leftmost 44A), third node (44A second from the left),
and fourth node (44B second from the left), the second node being in gated electrical
connection with the first node through the first wordline, and the fourth node being in
gated electrical connection with the third node through the second wordline;

defining a first, second, third, and fourth diffusion regions, the first diffusion
region (44B) being associated with the first node, the second diffusion (44A) region
being associated with the second node, the third diffusion region (44B) being associated

with the third node, and the fourth diffusion region being associated with the fourth node;

defining an isolation region (32) between the first wordline and the second wordline, the isolation region electrically isolating the first and second wordlines from each other;

forming a pair of spacers (42) along opposing sidewalls of each wordline, the first and second diffusion regions extending an initial distance under the first wordline, and the third and fourth regions extending an initial distance under the second wordline.

Hsiao et al. does not disclose the method of extending the first diffusion region farther under the first wordline relative to the initial distance without extending the second diffusion region.

Huster et al. disclose the method of extending the first diffusion region (120) farther under the first wordline relative to the initial distance without extending the second diffusion region (see Figure 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to extend the first diffusion region (source side of gate) farther under the first wordline relative to the initial distance without extending the second diffusion region because, as Huster et al. teach, the asymmetric doping profile allows for increase drain current, and higher operational speeds (see column 1, lines 40-45).

In re claim 54, the combined Hsiao et al. and Huster et al. disclose the method comprising extending the fourth diffusion region (source side of gate) farther under the second wordline relative to the initial distance without extending the third diffusion region. The examiner notes that Hsiao et al. teach that the fourth diffusion region corresponds to the source side and Huster et al. teach that the source side region (120) is doped to extend farther under the wordline than the corresponding drain region. As stated above, it would have been obvious to one of ordinary skill in the art at the time the invention was made to extend the fourth diffusion region (source side of gate) farther under the second wordline relative to the initial distance without extending the third diffusion region because, as Huster et al. teach, the asymmetric doping profile allows for increase drain current, and higher operational speeds (see column 1, lines 40-45).

In re claim 55, the combined Hsiao et al. and Huster et al. disclose the method wherein the spacers comprise a spacer width and wherein the initial distance is less than the spacer width (see Hsiao et al., Figure 5).

In re claim 56, the combined Hsiao et al. and Huster et al. disclose the method wherein in each of the diffusion regions are conductively doped with a first type dopant and wherein the extending comprises halo implanting a second type dopant (see Huster et al. column 3, lines 17-35).

In re claim 57, the combined Hsiao et al. and Huster et al. disclose the method wherein the diffusion regions are majority doped with n-type dopant and wherein the

extending comprises forming extension regions majority doped with p-type dopant (see Huster et al. column 3, lines 17-35).

In re claim 59, the combined Hsiao et al. and Huster et al. disclose the method further comprising forming a first and second capacitor constructions (52, 54, 56), the first capacitor construction being in electrical connection with the second node (left most capacitor), and the second capacitor construction being in electrical connection with the third node (capacitor second from the left), and forming a first bit line contact (leftmost 64, 66) in electrical connection with the first node and a second bit line contact in electrical connection with the third node (64, 66) second from the left (see Hsiao et al. column 5, lines 59-67 and Figure 12).

Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (U.S. Patent No. 5,946,568) and Huster et al. (U.S. Patent No. 6,242,329) in view of Huang (U.S. Patent No. 6,187,624).

In re claim 58, the combined Hsiao et al. and Huster et al. disclose the method as claimed and rejected above including forming the isolation region of Hsiao et al. of a field oxide layer, but do not disclose the method wherein the isolation region comprises a shallow trench isolation region.

Huang teaches that an isolation region between gates may be formed of either a field oxide layer or shallow trench isolation (see column 2, lines 55-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

form the isolation of the combined Hsiao et al. and Huster et al. with shallow trench isolation because as Huang teaches field oxide isolation and shallow trench isolation are interchangeable in the art to form isolation between gates, and because shallow trench isolation has improved planarity over field oxide isolation and also does not have the problems with bird's beak encroachment that is common in field oxide isolation.

Claims 60-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao et al. (U.S. Patent No. 5,946,568) and Huster et al. (U.S. Patent No. 6,242,329) in view of Iwamatsu et al. (U.S. Patent No. 5,440,161).

In re claims 60 and 61, the combined Hsiao et al. and Huster et al. disclose the method as claimed and rejected above, but do not disclose the method wherein the defining an isolation region comprises forming a doped pocket region (22a) within the semiconductor substrate, the doped pocket region comprising a pocket width, and forming an isolation mass (16, 17) over the substrate and over the pocket region, the isolation mass having a total mass width that is greater than the pocket width (see Figure 3 and column 12, lines 19-50) and wherein the isolation mass comprises a gate stack over the substrate, the gate stack having opposing sidewalls, a pair of insulative spacers (17) along the opposing sidewalls the total mass width being a distance between outer edges of the pair of insulative spacers measured at a surface of the substrate, and wherein the total mass width is at least about double the pocket width (see Figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the isolation region with an isolation gate as Iwamatsu et al. does because the isolation gate allows for isolation between elements and allows for independent control of threshold voltage compared to that of field oxide and shallow trench isolation.

The examiner maintains that Figure 3 shows that the total mass width is at least about double the pocket width. However, the examiner also notes that Applicant does not teach that the relative widths of the total mass width and the pocket width solves any stated problem or are for any particular purpose. Therefore, forming the total mass width to be at least about double the pocket width lacks criticality in the claimed invention and does not produce unexpected or novel results. Thus, it would have been obvious matter of design choice to form the total mass width to be at least about double the pocket width since it would have allowed for the channel dopant to be spaced apart from the source drain region while allowing for increased threshold voltage of the field shield transistor, thus improving the isolation capability of the device and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233, MPEP 2144.05 II A.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Divakuruni et al. (U.S. Patent No. 6,420,749) discloses the advantages of isolation gates over shallow trench isolation and field oxide isolation. Lin et al. (U.S. Patent No. 6,001,707) and Shiozawa et al. (U.S. Patent No. 5,970,352) disclose the advantages of STI over field oxide isolation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk